



**LGDP4532**

*a-Si TFT LCD Single Chip Driver with 240RGBx320 Resolution and 260K color*

# ***LGDP 4532***

## ***Application Note***

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written by LG SIC  
Version 1.0  
2007-07-02

Application Note Revision History

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*Index*

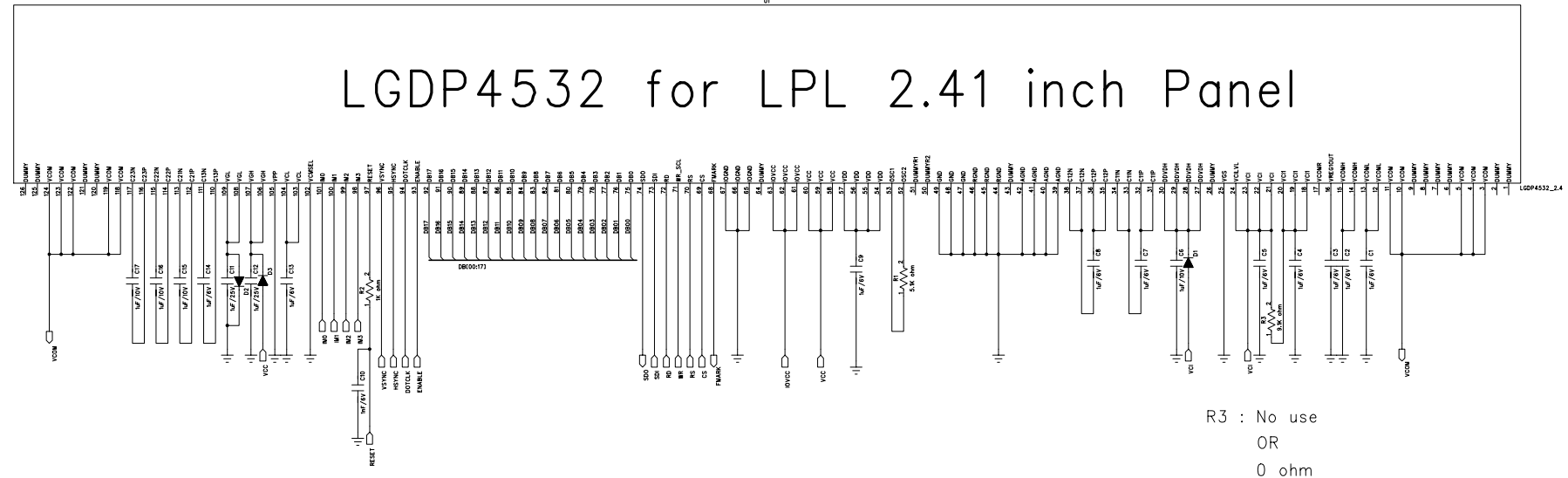


**1. LPL 2.41 inch panel FPC Circuit & initial code**

6 5 4 3 2 1

REVISION RECORD			
LTN	ECD NO.	APPROVED	DATE

# LGDP4532 for LPL 2.41 inch Panel



R3 : No use  
OR  
0 ohm

IM3	IM2	IM1	IM0/ID	Interface Mode
1	0	1	0	18-Bit Interface
0	0	1	0	16-Bit Interface
1	0	1	1	9-Bit Interface
0	0	1	1	8-Bit Interface
0	1	0	ID	Serial Peripheral Interface(SPI)

Note :

- 1) When the RGB interface is not used, please shorted the VSYNC, HSYNC, DOTCLK and ENABLE to GND.
- 2) When the SPI interface is not used, the SDI is shorted to GND and let SDO as open.
- 3) All the VCOM pins must be shorted together.
- 4) R3 : no use or 0 ohm

DRAWN: Su-Min Kim		DATED: 2007-06-20	
CHECKED: Vino Park		DATED: 2007-06-22	
QUALITY CONTROL:	DATED:	CODE:	SIZE:
RELEASED:	DATED:	SCALE:	SHEET: OF

COMPANY: **LG Electronics**  
TITLE: **LGDP4532 Application Circuit -LPL 2.41 inch**



# LG Electronics

Gamma Setting – LGDP4532 / LPL 2.41–inch module

Initial Code – LGDP4532 / LPL 2.41" for hand phone

\* Condition

1. VCI = VCC = IOVCC = 2.8V
2. External resistor of OSC = 5.1K ohm
3. R90 [DIV1] = "01" => 1/2 division

Initialization		
Reg (Hex)	Data (Hex)	Delay (ms)
0X15	0X0030	
0X11	0X0040	
0X10	0X1628	
0X12	0X0000	
0X13	0X1047	
DELAY		40
0X12	0X0010	
DELAY		40
0X10	0X2820	
0X13	0X304F	
DELAY		20
0X30	0X0000	
0X31	0X0402	
0X32	0X0106	
0X33	0X0503	
0X34	0X0104	
0X35	0X0301	
0X36	0X0707	
0X37	0X0305	
0X38	0X0208	
0X39	0X0F0B	
0X01	0X0100	
0X02	0X0300	
0X03	0X1030	
0X08	0X0604	
0X09	0X0000	
0X0A	0X0000	
0X17	0X0770	
0X41	0X0002	
0X60	0X2700	
0X61	0X0001	
0X90	0X0199	
0X93	0X0001	
0X07	0X0001	
0X07	0X0021	
0X07	0X0023	
0X07	0X0033	
0X07	0X0133	

Power ON sequence

Display Mode & Gamma settings

Display ON sequence

SLEEP ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0132	
DELAY		20
0X07	0X0122	
DELAY		20
0X07	0X0102	
DELAY		20
0X07	0X0000	
DELAY		10
0X10	0X0000	
0X12	0X0000	
0X13	0X0000	
DELAY		10
0X10	0X0002	

STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0132	
DELAY		20
0X07	0X0122	
DELAY		20
0X07	0X0102	
DELAY		20
0X07	0X0000	
DELAY		10
0X10	0X0000	
0X12	0X0000	
0X13	0X0000	
DELAY		10
0X10	0X0001	

DEEP STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0132	
DELAY		20
0X07	0X0122	
DELAY		20
0X07	0X0102	
DELAY		20
0X07	0X0000	
DELAY		10
0X10	0X0000	
0X12	0X0000	
0X13	0X0000	
DELAY		10
0X10	0X0004	

SLEEP EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X10	0X0008	
↓		
Power ON sequence		
↓		
Display ON sequence		

STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X10	0X0008	
↓		
Power ON sequence		
↓		
Display ON sequence		

DEEP STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
6 times CS pin toggle or RESET		
DELAY		20
Initialization		



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